Invariance of S_{21}/S_{12} and K-Factor under Parallel Operation of Linear Two-Port Devices

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Abstract—**Based on a generalized circuit model for parallel-operated amplifiers with linear two-port devices, it has been proved that the S-parameter ratio S_{21}/S_{12} and hence MSG (Maximum Stable Gain) are invariant as long as the devices have an identical value of S_{21}/S_{12} and the input and output networks are reciprocal. The invariance of K-factor has been shown to hold for two cases: (i) devices are identical and input/output networks are lossless and symmetric with respect to each device, and (ii) identical admittances are added to the networks of case (i) so as to connect every device port with each other. Thus at least in these two cases, MAG (Maximum Available Gain) and U (Unilateral Gain) are invariant as well as MSG under parallel operation of linear two-port devices. The invariance of S_{21}/S_{12} and hence MSG applies to a variety of parallel-operated amplifiers such as distributed amplifiers and linear power amplifiers.**

I. Introduction

MSG, MAG, and U are the parameters indicating the performance level of a linear two-port device or amplifier circuit, and are given in terms of S-parameters and K-factor of the device or the circuit as [1]

$$\mathrm{MSG} = |S_{21}/S_{12}|$$
$$\mathrm{MAG} = \mathrm{MSG}/\left(K + \sqrt{K^2 - 1}\right)$$
$$\mathrm{U} = \frac{|S_{21}/S_{12} - 1|^2}{2K|S_{21}/S_{12}| - 2\,\mathrm{Re}(S_{21}/S_{12})}\,.$$

To build an amplifier, the device is imbedded in a circuit cascaded with reciprocal input and output networks. The MSG of the amplifier is unaffected by input and output parasitics [1]. Actually the ratio S_{21}/S_{12} is invariant as can easily be seen from the facts that the overall T-matrix of a cascaded linear two-port network chain is given by multiplying individual T-matrices and that the determinant of T-matrix is equal to S_{21}/S_{12} [2]. Meanwhile the K-factor of the amplifier is equal to or larger than that of the device depending on whether the input and output networks are lossless or not [3]. Thus contrary to MSG, MAG and U of the amplifier become smaller than that of the device for lossy input and output networks.

In distributed amplifiers and some types of power amplifiers, multiple two-port devices are connected in parallel via reciprocal networks such as hybrids and distributed lines. These amplifiers can generally be represented by an equivalent circuit as shown in Fig. 1, where m two-port devices ($\#1 - \#m$) are imbedded in parallel between n-port reciprocal networks A and B, where $n = m + 1$. It is then of interest to examine whether invariant properties as in the single-device amplifier exist or not.

This paper addresses the invariance of S_{21}/S_{12} in the generalized parallel-operated amplifier and shows that, if each device has an equal value of S_{21}/S_{12}, the S_{21}/S_{12} of the amplifier is equal to that of the devices. It is also shown that the K-factor is invariant, if each device is identical and the networks A and B are lossless and symmetric with respect to each device. Addition of identical admittances connecting every device port with each other also leaves the K-factor invariant.

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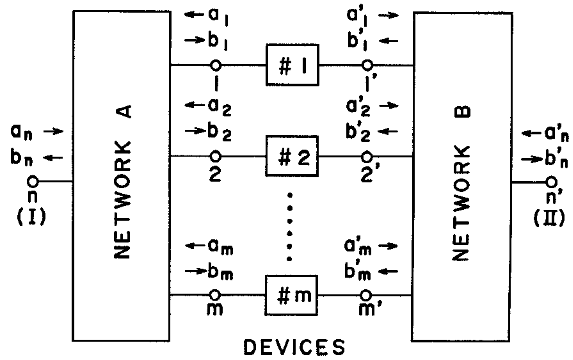

Fig. 1. Generalized equivalent circuit of parallel-operated multi-device amplifier, where $\#1 - \#m$ are linear two-port devices, networks A and B reciprocal n-ports, (a_i, b_i) and (a_i', b_i') incident and reflected waves at port i and i' $(1 \leqq i \leqq n)$, and $n = m + 1$.

II. Invariance of S_{21}/S_{12} Under Parallel Operation

If S_{21}/S_{12} of the devices in Fig. 1 has an identical value denoted here by γ, it can then be shown that S_{21}/S_{12} of the two-port regarding ports n and n' as ports 1 and 2, respectively, is also equal to γ.

Proof: Let $\boldsymbol{S_A}$ and $\boldsymbol{S_B}$ be the $n \times n$ S-matrices of network A and network B, with ij component S_{Aij} and S_{Bij}, respectively. $\boldsymbol{S_A}$ and $\boldsymbol{S_B}$ can then be represented by

$$\boldsymbol{S_A} = \left[\begin{array}{c|c} \boldsymbol{S_{Am}} & \boldsymbol{s_A^T} \\ \hline \boldsymbol{s_A} & S_{Ann} \end{array}\right] \quad \text{and}$$

$$\boldsymbol{S_B} = \left[\begin{array}{c|c} \boldsymbol{S_{Bm}} & \boldsymbol{s_B^T} \\ \hline \boldsymbol{s_B} & S_{Bnn} \end{array}\right],$$

where

$$(\boldsymbol{S_{Am}})_{i,j} = S_{Aij}, \qquad 1 \leqq i, \quad j \leqq m,$$
$$(\boldsymbol{S_{Bm}})_{i,j} = S_{Bij}, \qquad 1 \leqq i, \quad j \leqq m,$$
$$\boldsymbol{s_A} = [S_{A1n}, S_{A2n}, \cdots, S_{Amn}],$$
$$\boldsymbol{s_B} = [S_{B1n}, S_{B2n}, \cdots, S_{Bmn}],$$

and the superscript T indicates the transpose of a matrix. Note that $\boldsymbol{S_A}$ and $\boldsymbol{S_B}$, hence $\boldsymbol{S_{Am}}$ and $\boldsymbol{S_{Bm}}$, are symmetric matrices. Denoting the S-matrix of the kth device $(1 \leqq k \leqq m)$ as

$$\begin{bmatrix} S_{D11}^{(k)} & S_{D12}^{(k)} \\ S_{D21}^{(k)} & S_{D22}^{(k)} \end{bmatrix},$$

we define diagonal matrices $\boldsymbol{S_{D11}}$, $\boldsymbol{S_{D12}}$, $\boldsymbol{S_{D21}}$, and $\boldsymbol{S_{D22}}$ by

$$\boldsymbol{S_{Dij}} = \mathrm{diag}\left[S_{D\,ij}^{(1)}, S_{D\,ij}^{(2)}, \cdots, S_{D\,ij}^{(m)}\right], \qquad 1 \leqq \mathrm{i, j} \leqq 2$$

where $S_{Dij}^{(1)}$, $S_{Dij}^{(2)}$, $\cdots$ are diagonal components.

Let the incident and reflected waves at port i of network A and at port i' of network B be (a_i, b_i) and (a_i', b_i'), respectively. Then from the definition of S-matrix, we have

$$\boldsymbol{b_m} = \boldsymbol{S_{Am}a_m} + a_n\boldsymbol{s_A^T}, \tag{1}$$

$$\boldsymbol{b_m'} = \boldsymbol{S_{Bm}a_m'} + a_n'\boldsymbol{s_B^T}, \tag{2}$$

$$b_n = \boldsymbol{s_A a_m} + a_n S_{Ann}, \tag{3}$$

$$b'_n = \boldsymbol{s_B a'_m} + a'_n S_{Bnn}, \tag{4}$$

$$\boldsymbol{a_m} = \boldsymbol{S_{D11} b_m} + \boldsymbol{S_{D12} b'_m}, \tag{5}$$

$$\boldsymbol{a'_m} = \boldsymbol{S_{D21} b_m} + \boldsymbol{S_{D22} b'_m}, \tag{6}$$

where

$$\boldsymbol{a_m} = [a_1, a_2, \cdots, a_m]^T,$$
$$\boldsymbol{b_m} = [b_1, b_2, \cdots, b_m]^T,$$
$$\boldsymbol{a'_m} = [a'_1, a'_2, \cdots, a'_m]^T,$$
$$\boldsymbol{b'_m} = [b'_1, b'_2, \cdots, b'_m]^T.$$

By substituting (1) and (2) into (5) and (6), we have

$$(\boldsymbol{S_{D11} S_{Am}} - \boldsymbol{I})\boldsymbol{a_m} + \boldsymbol{S_{D12} S_{Bm} a'_m} = -a_n \boldsymbol{S_{D11} s_A^T} - a'_n \boldsymbol{S_{D12} s_B^T}, \tag{7}$$

$$\boldsymbol{S_{D21} S_{Am} a_m} + (\boldsymbol{S_{D22} S_{Bm}} - \boldsymbol{I})\boldsymbol{a'_m} = -a_n \boldsymbol{S_{D21} s_A^T} - a'_n \boldsymbol{S_{D22} s_B^T} \tag{8}$$

where $\boldsymbol{I}$ is the $m \times m$ identity matrix. Equations (7) and (8) can then be solved for $\boldsymbol{a_m}$ and $\boldsymbol{a'_m}$ to give

$$\boldsymbol{a_m} = a_n \boldsymbol{F G s_A^T} + a'_n \boldsymbol{F s_B^T}, \tag{9}$$

$$\boldsymbol{a'_m} = a_n \boldsymbol{F' s_A^T} + a'_n \boldsymbol{F' G' s_B^T}, \tag{10}$$

where

$$\boldsymbol{F} = \Big[(\boldsymbol{S_{Bm} S_{D22}} - \boldsymbol{I})\boldsymbol{S_{D12}^{-1}}(\boldsymbol{S_{D11} S_{Am}} - \boldsymbol{I}) - \boldsymbol{S_{Bm} S_{D21} S_{Am}}\Big]^{-1},$$
$$\boldsymbol{G} = \boldsymbol{S_{Bm} S_{D21}} - (\boldsymbol{S_{Bm} S_{D22}} - \boldsymbol{I})\boldsymbol{S_{D12}^{-1} S_{D11}},$$
$$\boldsymbol{F'} = \Big[(\boldsymbol{S_{Am} S_{D11}} - \boldsymbol{I})\boldsymbol{S_{D21}^{-1}}(\boldsymbol{S_{D22} S_{Bm}} - \boldsymbol{I}) - \boldsymbol{S_{Am} S_{D12} S_{Bm}}\Big]^{-1},$$
$$\boldsymbol{G'} = \boldsymbol{S_{Am} S_{D12}} - (\boldsymbol{S_{Am} S_{D11}} - \boldsymbol{I})\boldsymbol{S_{D21}^{-1} S_{D22}}.$$

Substitution of (9) and (10) into (3) and (4) finally yields

$$b_n = S_{\mathrm{I\,I}} a_n + S_{\mathrm{I\,II}} a'_n,$$
$$b'_n = S_{\mathrm{II\,I}} a_n + S_{\mathrm{II\,II}} a'_n,$$

where $S_{\mathrm{I\,I}}$, $S_{\mathrm{I\,II}}$, $S_{\mathrm{II\,I}}$, and $S_{\mathrm{II\,II}}$ are the S-parameters of the two-port with port I (port n) and port II (port n′), and given by

$$S_{\mathrm{I\,I}} = S_{Ann} + \boldsymbol{s_A F G s_A^T},$$
$$S_{\mathrm{I\,II}} = \boldsymbol{s_A F s_B^T}, \tag{11}$$

$$S_{\mathrm{II\,I}} = \boldsymbol{s_B F' s_A^T} = \boldsymbol{s_A F'^T s_B^T},$$
$$S_{\mathrm{II\,II}} = S_{Bnn} + \boldsymbol{s_B F' G' s_B^T}. \tag{12}$$

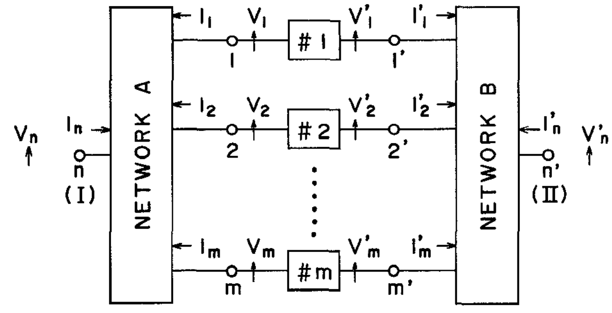

Fig. 2. Generalized equivalent circuit of Fig. 1 showing voltage and current definition at each port.

If $S_{D21}^{(1)}/S_{D12}^{(1)} = S_{D21}^{(2)}/S_{D12}^{(2)} = \cdots = S_{D21}^{(m)}/S_{D12}^{(m)} = \gamma$ holds, i.e. $\boldsymbol{S_{D21}} = \gamma \boldsymbol{S_{D12}}$, we have

$$\boldsymbol{F'^T} = \Big[(\boldsymbol{S_{Bm} S_{D22}} - \boldsymbol{I})\boldsymbol{S_{D21}^{-1}}(\boldsymbol{S_{D11} S_{Am}} - \boldsymbol{I}) - \boldsymbol{S_{Bm} S_{D12} S_{Am}}\Big]^{-1} = \gamma \boldsymbol{F}.$$

Hence form (11) and (12) we obtain

$$S_{\mathrm{II\,I}}/S_{\mathrm{I\,II}} = \gamma, \tag{13}$$

which completes the proof.

III. Invariance of K-Factor Under Parallel Operation

Invariance of K-factor under parallel operation of identical devices is shown in the following two cases. In case 1, the reciprocal networks A and B are assumed to be lossless and symmetric with respect to ports 1-m and $1'$-m'. In case 2, identical admittances are added to the networks A and B of case 1, respectively, so as to connect every port of 1-m and $1'$-m' with each other.

To facillitate the analysis, Y-parameter representation is used. From (A1)–(A6) in the Appendix that relate port currents and voltages defined in Fig. 2, the Y-parameters of the two-port regarding ports n and n' in Fig. 2 as ports I and II, respectively, can be derived in a similar procedure as in Section II, giving

$$Y_{\mathrm{I\,I}} = Y_{Ann} - \boldsymbol{y_A P Q y_A^T},$$
$$Y_{\mathrm{I\,II}} = \boldsymbol{y_A P y_B^T}, \tag{14}$$

$$Y_{\mathrm{II\,I}} = \boldsymbol{y_B P' y_A^T},$$
$$Y_{\mathrm{II\,II}} = Y_{Bnn} - \boldsymbol{y_B P' Q' y_B^T}. \tag{15}$$

where

$$\boldsymbol{P} = \Big[(\boldsymbol{Y_{D22}} + \boldsymbol{Y_{Bm}})\boldsymbol{Y_{D12}^{-1}}(\boldsymbol{Y_{D11}} + \boldsymbol{Y_{Am}}) - \boldsymbol{Y_{D21}}\Big]^{-1},$$
$$\boldsymbol{Q} = (\boldsymbol{Y_{D22}} + \boldsymbol{Y_{Bm}})\boldsymbol{Y_{D12}^{-1}},$$
$$\boldsymbol{P'} = \big[(\boldsymbol{Y_{D11}} + \boldsymbol{Y_{Am}})\boldsymbol{Y_{D21}^{-1}}(\boldsymbol{Y_{D22}} + \boldsymbol{Y_{Bm}}) - \boldsymbol{Y_{D12}}\big]^{-1},$$
$$\boldsymbol{Q'} = (\boldsymbol{Y_{D11}} + \boldsymbol{Y_{Am}})\boldsymbol{Y_{D21}^{-1}}.$$

The definitions of the right-hand-side matrices in the above equations are given in the Appendix. Note that $Y_{\mathrm{II\,I}}/Y_{\mathrm{I\,II}} = \gamma$ if $\boldsymbol{Y_{D21}} = \gamma \boldsymbol{Y_{D12}}$, being consistent with (13).

Now let us assume in the following that the devices (#1 − #m) are identical. Denoting $Y_{Dij}^{(k)} = Y_{Dij}$ for $1 \leqq k \leqq m$, we have

$$\boldsymbol{Y_{Dij}} = Y_{Dij}\boldsymbol{I}, \qquad 1 \leqq i, \qquad j \leqq 2.$$

Case 1: If the networks A and B in Fig. 2 are assumed to be symmetric with respect to ports 1-m and $1'$-m', we have

$$
\begin{aligned}
&Y_{Aii} = Y_{A\lambda}, && Y_{Bii} = Y_{B\lambda}, && 1 \leqq i \leqq m,\\
&Y_{Aij} = Y_{A\mu}, && Y_{Bij} = Y_{B\mu}, && 1 \leqq i \neq j \leqq m,\\
&Y_{Ain} = Y_{A\nu}, && Y_{Bin} = Y_{B\nu}, && 1 \leqq i \leqq m.
\end{aligned}
$$

After some lengthy calculation, the components of the m × m matrices, $\boldsymbol{P}$ and $\boldsymbol{Q}$, are calculated to be

$$
(\boldsymbol{P})_{i,i} = Y_{D12}[s + (m-2)t]/\{(s-t)[s+(m-1)t]\}, \quad 1 \leqq i \leqq m, \tag{16}
$$

$$
(\boldsymbol{P})_{i,j} = -Y_{D12}t/\{(s-t)[s+(m-1)t]\}, \qquad 1 \leqq i \neq j \leqq m, \tag{17}
$$

$$
(\boldsymbol{Q})_{i,i} = Y_{D12}^{-1}[Y_{D22} + Y_{B\lambda}], \qquad 1 \leqq i \leqq m, \tag{18}
$$

$$
(\boldsymbol{Q})_{i,j} = Y_{D12}^{-1}Y_{B\mu}, \qquad 1 \leqq i \neq j \leqq m, \tag{19}
$$

where

$$
\begin{aligned}
s &= Y_{D11}Y_{D22} - Y_{D12}Y_{D21} + Y_{D22}Y_{A\lambda} + Y_{D11}Y_{B\lambda}\\
&\quad + Y_{A\lambda}Y_{B\lambda} + (m-1)Y_{A\mu}Y_{B\mu}\\
t &= Y_{A\lambda}Y_{B\mu} + Y_{A\mu}Y_{B\lambda} + Y_{D22}Y_{A\mu} + Y_{D11}Y_{B\mu}\\
&\quad + (m-2)Y_{A\mu}Y_{B\mu}.
\end{aligned}
$$

Substituting (16)–(19) into (14) and (15), we finally obtain

$$
Y_{\mathrm{I\,I}} = Y_{Ann} - mY_{A\nu}^2[Y_{D22} + Y_{B\lambda} + (m-1)Y_{B\mu}]/D, \tag{20}
$$

$$
Y_{\mathrm{I\,II}} = mY_{A\nu}Y_{B\nu}Y_{D12}/D \tag{21}
$$

where

$$
\begin{aligned}
D = s + (m-1)t &= [Y_{D11} + Y_{A\lambda} + (m-1)Y_{A\mu}]\\
&\quad \cdot [Y_{D22} + Y_{B\lambda} + (m-1)Y_{B\mu}]\\
&\quad - Y_{D12}Y_{D21}.
\end{aligned}
$$

Similarly we obtain

$$
Y_{\mathrm{II\,I}} = mY_{A\nu}Y_{B\nu}Y_{D21}/D, \tag{22}
$$

$$
Y_{\mathrm{II\,II}} = Y_{Bnn} - mY_{B\nu}^2[Y_{D11} + Y_{A\lambda} + (m-1)Y_{A\mu}]/D. \tag{23}
$$

Then it can be shown that the two-port with Y-parameters given by (20)–(23) is equivalent to the cascaded circuit in Fig. 3, where network I, device, and network II, have Y-matrices $[\boldsymbol{Y}_{\mathrm{I}}]$, $[\boldsymbol{Y}_D]$ and $[\boldsymbol{Y}_{\mathrm{II}}]$, respectively, with the definitions given in the same figure.

If we assume that the networks A and B in Fig. 2 are lossless, their Y-matrices are pure imaginary, and so are $[\boldsymbol{Y}_{\mathrm{I}}]$ and $[\boldsymbol{Y}_{\mathrm{II}}]$, indicating that the networks I and II in Fig. 3 are also lossless. Hence the K-factor is left invariant as in the single-device amplifier [3].

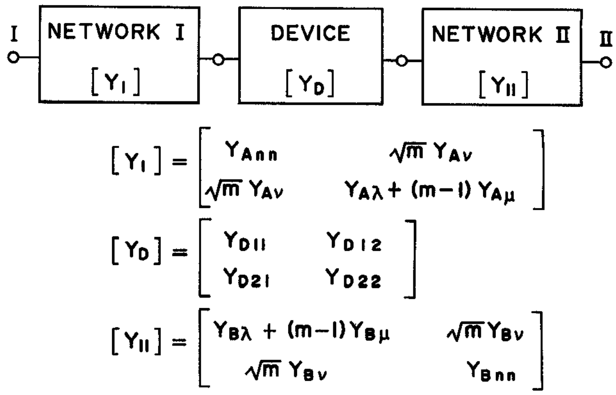

Fig. 3. Equivalent circuit of Fig. 2 when devices are identical and networks A and B are symmetric with respect to each device. Y-matrices of network I, device, and network II are also shown.

Case 2: Let us consider a case in which admittances, Y_{AS} and Y_{BS} are added to modify the networks A and B of case 1 so that every port i and i' ($1 \leqq i \leqq m$) is connected via Y_{AS} and Y_{BS} with every other port j and j' ($1 \leqq j \leqq m, j \neq i$), respectively. Here Y_{AS} and Y_{BS} need not be pure susceptance. Then the Y-parameters of the modified networks A and B, Y'_{Aij} and Y'_{Bij}, are given by

$$
\begin{aligned}
&Y'_{Aii} = Y'_{A\lambda} = Y_{A\lambda} + (m-1)Y_{AS}, \qquad 1 \leqq i \leqq m,\\
&Y'_{Bii} = Y'_{B\lambda} = Y_{B\lambda} + (m-1)Y_{BS}, \qquad 1 \leqq i \leqq m,\\
&Y'_{Aij} = Y'_{A\mu} = Y_{A\mu} - Y_{AS}, \qquad 1 \leqq i \neq j \leqq m,\\
&Y'_{Bij} = Y'_{B\mu} = Y_{B\mu} - Y_{BS}, \qquad 1 \leqq i \neq j \leqq m,\\
&Y'_{Ain} = Y'_{A\nu} = Y_{A\nu}, \qquad Y'_{Bin} = Y'_{B\nu} = Y_{B\nu}, \qquad 1 \leqq i \leqq m.\\
&Y'_{Ann} = Y_{Ann}, \qquad Y'_{Bnn} = Y_{Bnn}.
\end{aligned}
$$

The Y-matrices $[\boldsymbol{Y}_{\mathrm{I}}]$ and $[[\boldsymbol{Y}_{\mathrm{II}}]$ corresponding to Y'_{Aij} and Y'_{Bij} are pure imaginary as in case 1, since

$$
\begin{aligned}
Y'_{A\lambda} + (m-1)Y'_{A\mu} &= Y_{A\lambda} + (m-1)Y_{A\mu},\\
Y'_{B\lambda} + (m-1)Y'_{B\mu} &= Y_{B\lambda} + (m-1)Y_{B\mu},
\end{aligned}
$$

where we can see that Y_{AS} and Y_{BS} cancel out and do not appear on the right-hand sides. Therefore the invariance of K-factor also holds as in case 1.

IV. Conclusion

It has been proved that S_{21}/S_{12} (hence MSG) is invariant under parallel operation of linear two-port devices as long as the devices have an identical value of S_{21}/S_{12} and the input and output networks are reciprocal. Since the input/output networks need not be lossless, such invariance holds for a variety of parallel-operated amplifiers such as distributed amplifiers and linear power amplifiers. Meanwhile invariance of K-factor has been proved only in two cases: (i) identical devices and lossless input/output networks symmetric with respect to each device, and (ii) addition of identical admittances connecting every device port with each other. Thus at least in these two idealized cases MAG and U are invariant as well as MSG under parallel operation of linear two-port devices. In practical amplifiers device and circuit parameter variations are, more or less, unavoidable. Further work on how these variations affect MSG, MAG and U is still needed.

V. Appendix

Let the Y-parameters of networks A and B in Fig. 2 be

$$\boldsymbol{Y_A} = \left[\begin{array}{c|c} \boldsymbol{Y_{Am}} & \boldsymbol{y_A^T} \\ \hline \boldsymbol{y_A} & Y_{Ann} \end{array}\right] \quad \text{and}$$

$$\boldsymbol{Y_B} = \left[\begin{array}{c|c} \boldsymbol{Y_{Bm}} & \boldsymbol{y_B^T} \\ \hline \boldsymbol{y_B} & Y_{Bnn} \end{array}\right],$$

respectively, where

$$(\boldsymbol{Y_{Am}})_{i,j} = Y_{Aij}, \qquad (\boldsymbol{Y_{Bm}})_{i,j} = Y_{Bij},$$
$$1 \leqq i, \qquad j \leqq m,$$
$$\boldsymbol{y_A} = [Y_{A1n}, Y_{A2n}, \cdots, Y_{Amn}],$$
$$\boldsymbol{y_B} = [Y_{B1n}, Y_{B2n}, \cdots, Y_{Bmn}].$$

Denoting the Y-matrix of the k-th device $(1 \leqq k \leqq m)$ as

$$\begin{bmatrix} Y_{D11}^{(k)} & Y_{D12}^{(k)} \\ Y_{D21}^{(k)} & Y_{D22}^{(k)} \end{bmatrix},$$

we define matrices $\boldsymbol{Y_{D11}}$, $\boldsymbol{Y_{D12}}, \boldsymbol{Y_{D21}}$, and $\boldsymbol{Y_{D22}}$ by

$$\boldsymbol{Y_{Dij}} = \text{diag}\left[Y_{Dij}^{(1)}, Y_{Dij}^{(2)}, \cdots, Y_{Dij}^{(m)}\right], \qquad 1 \leqq i, \qquad j \leqq 2.$$

Then we obtain six equations similar to (1)–(6) in the text:

$$\boldsymbol{I_m} = \boldsymbol{Y_{Am}} \boldsymbol{V_m} + V_n \boldsymbol{y_A^T}, \tag{A1}$$

$$\boldsymbol{I'_m} = \boldsymbol{Y_{Bm}} \boldsymbol{V'_m} + V'_n \boldsymbol{y_B^T}, \tag{A2}$$

$$I_n = \boldsymbol{y_A} \boldsymbol{V_m} + V_n Y_{Ann}, \tag{A3}$$

$$I'_n = \boldsymbol{y_B} \boldsymbol{V'_m} + V'_n Y_{Bnn}, \tag{A4}$$

$$\boldsymbol{I_m} = -\boldsymbol{Y_{D11}} \boldsymbol{V_m} - \boldsymbol{Y_{D12}} \boldsymbol{V'_m}, \tag{A5}$$

$$\boldsymbol{I'_m} = -\boldsymbol{Y_{D21}} \boldsymbol{V_m} - \boldsymbol{Y_{D22}} \boldsymbol{V'_m}, \tag{A6}$$

where

$$\boldsymbol{I_m} = [I_1, I_2, \cdots, I_m]^T,$$
$$\boldsymbol{I'_m} = [I'_1, I'_2, \cdots, I'_m]^T,$$
$$\boldsymbol{V_m} = [V_1, V_2, \cdots, V_m]^T,$$
$$\boldsymbol{V'_m} = [V'_1, V'_2, \cdots, V'_m]^T.$$

From (A1)–(A6), the Y-parameters $(Y_{\rm I\,I}, Y_{\rm I\,II}, Y_{\rm II\,I}, Y_{\rm II\,II})$ in the text can be obtained.

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A Model for Coplanar Waveguide Transmission Line Structures on Semiconductor Substrates

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Abstract—**An accurate model for coplanar waveguide transmission line structures on semiconductive substrates is presented. The model is useful for simulating long (> 0.5 mm) interconnects on LSI and VLSI GaAs circuits as well as high speed Si ICs. When simulated in the frequency domain, the model shows an excellent match to measured S parameters of coplanar waveguide samples.**

I. Introduction

Since most GaAs integrated circuits are fabricated on semi-insulating substrates, the parasitic capacitances of interconnect lines to the backside RF ground plane are low. However, trends toward high density digital GaAs circuits result in closely spaced lines, and the interconnect parasitic capacitances from line to line are far more significant than those from line to distant ground plane. This would prompt us to treat long interconnects as coplanar waveguide (CPW) transmission lines, not as microstrip transmission lines [1]. The CPW lines are isolated from the back side ground plane and exhibit a quasi-TEM mode of propagation. Furthermore, in cases in which well controlled impedance characteristics are required, CPW lines can be produced by placing ground conductors adjacent to the signal lines.

A four element RLGC model is usually accurate for modelling CPW structures on semi-insulating GaAs, but not accurate when the structures are above a semiconductive substrate. Some digital GaAs MESFET processes, for example, incorporate p^- implants for threshold voltage control. If the implant layer extends below interconnect lines, as it would if the implant is not a selective one, signal propagation will be affected adversely by the presence of a lossy plane in close proximity to signal lines. This effect must be included in an accurate model.

This letter presents an accurate, physically intuitive model for simulating CPW structures above semiconductive substrates. The model is shown to be far superior to the simple four element RLGC model and significantly better than the model of reference [2].

II. Measurements and Analysis

The test structures used for this study were 1 cm long CPW transmission lines whose cross section is depicted in Fig. 1. Line lengths were constrained to 1 cm by reticle size limitations. The samples were fabricated by Vitesse Semiconductor through the MOSIS foundry service [3]. The Vitesse process incorporates a nonselective

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